-

Table of Contents

Note : Remove “Table of Content” before including in CP Book
Each Course Plan shall be printed and made into a book with cover page
Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

the uses

CS
Prepared by Checked by Approved

18CS32 : ANALOG AND DIGITAL ELECTRONICS

A. COURSE INFORMATION

1. Course Overview

Degree:	B.E	Program:	CS
Year / Semester :	3	Academic Year:	2018
Course Title:	Analog and Digital Electronics	Course Code:	18CS33
Credit / L-T-P:	4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	50	SEE Marks:	60 Marks
CIA Marks:	30	Assignment	1 / Module
Course Plan Author:	Rashmi K T	Sign	Dt:
Checked By:		Sign	Dt:

2. Course Content

Module	Module Content	Teaching Hours	Module Concepts	Blooms Level
1	Field Effect Transistors: Junction Field Effect Transistors, MOSFETs,Differences between JFETs and MOSFETs Biasing MOSFETs, FET Applications, CMOS Devices. Wave-Shaping Circuits: Integrated Circuit(IC) Multivibrators. Introduction to Operational Amplifier: Ideal v/s practical Opamp, Performance Parameters,Amplifier Application Circuits :Peak Detector Circuit,Comparator, Active Filters,Non-Linear Amplifier, Relaxation Oscillator,Current-To-Voltage Converter Voltage-To-Current Converter.	10	FET Charecterstics OPAMP application circuits	L2
2	The Basic Gates: Review of Basic Logic gates, Positive and Negative Logic, Introduction to HDL. Combinational Logic Circuits: Sum-of-Products Method,Truth Table to Karnaugh Map, Pairs ,Quads, and Octets, Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, Product-of-sums simplifications, Simplification by Quine- McClusky Method, Hazards and Hazard covers, HDL Implementation Model	10	Logic gates fundamentals Boolean equation simplification	L2 L4
3	Data Processing Circuits: Multiplexers, Demultiplexer 1-of-16 Decoder, BCD to Decimal Decoders,Seven Segment Decoders, Encoders,Exclusive-OR Gates, Parity Generators and Checkers, Magnitude Comparator, Prog rammable Array Logic Programmable Logic Arrays, HDL Implementation of Data Processing Circuits. Arithmetic Building Blocks, Arithmetic Logic Unit,Flip- Flops: RS Flip-Flops, Gated Flip-Flops, Edge-triggered RS FLIP-FLOP, Edge-triggered D FLIP-FLOPs, Edge-triggered JK FLIP-FLOPs.	10	Data processing circuits design Flip flops Operation	L4 L2
4	Flip-Flops: FLIP-FLOP Timing, JK Master-slave FLIP-FLOP, SwitchContact Bounce Circuits, Various Representation of FLIP-FLOPs,HDL Implementation of FLIP-FLOP. Registers: Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In - Serial Out, Parallel In - Parallel Out, Universal Shift Register, Applications of Shift Registers, Register implementation in HDL Counters: Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus.	10	Flipflop representation Register and counter operation	L2
5	Counters: Decade Counters, Presettable Counters Counter Design as a Synthesis problem, A Digital Clock, Counter Design using HDL	10	Counter design	L4

	D/A Conversion and A/D Conversion: Variable, Resistor Networks, Binary Ladders, D/A Converters, D/A Accuracy and Resolution, A/D Converter-Simultaneous Conversion A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques, Dual-slope A/D Conversion, A/D Accuracy AND RESOLUTTION		Data conversion techniques	L2

3. Course Material

Module	Details	Available
	Text books	
1	Anil K Maini, Varsha Agarwal: Electronic Devicesand Circuits, Wiley, 2012.	In Lib
2-5	Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015	In Lib
	Reference books	
2-5	Stephen Brown, Zvonko Vranesic: Fundamentals of Digital Logic Design with VHDL, 2nd Edition, Tata McGraw Hill, 2005.	In dept
2-5	R D Sudhaker Samuel: Illustrative Approach to LogicDesign, Sanguine-Pearson, 2010	In dept
2-5	M Morris Mano: Digital Logic and Computer Design, 10th Edition, Pearson, 2008.	In dept
	Others (Web, Video, Simulation, Notes etc.)	
1-5	*https://www.tutorialspoint.com/*analog and digital electronics	Available
1-5	http://wwww.khanacademy.org/	

4. Course Prerequisites

SNo	Course Code	Course Name	Module / Topic / Description	Sem	Remarks	Blooms Level
1	18CS32	Analog and digital electronics	1/Knowledge 0f semiconductors	3		L2
2	18CS32	Analog and digital electronics	2 -5/Knowledge of number systems and boolean algebra	3		L2

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

B. OBE PARAMETERS

1. Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
	Student should be able to	-	-	-	-	-
18CS32.1	Understand the operation of Field effect transistors by V-I characteristics	5	FET charectersticS	Lecture	Q & A Unit test	L2 Understand
.2	Understand the operation amplifier	06	Operation	Lecture	Q & A	L2

	application circuits		amplifier application circuits	PPT	Unit test	
.3	Understand the fundamentals of logic gates through truth table	02	Logic Gates Fundamentals	Lecture	Assignment and Slip Test	L2
CO4	Simplify Boolean equations by Karnaugh map and Quine MCClusky method to design combinational circuits	08	Boolean equation simplification	Lecture / PPT	Slip test CIA	L4
CO5	Design data processing circuits using combination of gates	06	Data processing circuit design	Lecture	Slip test CIA	L4
CO6	Understand the fundamentals of flip flops by truth table and timing diagram	05	Flip flop fundamentals	Lecture and Tutorial	Assignment	L2
CO7	Represent the flip flops as state diagram, characteristic equation	04	Flip flop representation	Lecture	Assignment	L2
CO8	Illustrate the register and counter properties through truth table and timing diagram	06	Registers and counters properties	Lecture	Q & A CIA	L2
CO9	Design of mod n counters by combination of flip flops	04	Counter design	Lecture	Assignment CIA	L4
CO10	Interpret data conversion techniques through counter, continuous , dual slop methods	06	Data conversion techniques	Lecture PPT	Assignment CIA	L2
-	**Total**	**52**	-	-	-	-

Note: Identify a max of 2 Concepts per Module. Write 1 CO per concept.

2. Course Applications

SNo	Application Area	CO	Level
1	FETs are used as analog switches, amplifiers and current limiters	CO1	L2
2	Opamps are used for current to voltage converter, integrator	CO2	L2
3	Use of logic gates for building combinational circuits	CO3	L2
4	Used to simplification of boolean expressions	CO4	L4
5	Data processing circuits can be used in communication system	CO5	L4
6	Flip flops are used to store the data.	CO6	L2
7	Flip flops can be used as frequency divider	CO7	L4
8	Registers are used to store the instructions	CO8	L2
9	Counters are used for counting electronic pulses	CO9	L4
10	Used to convert signals	CO10	L4

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO1	PO2	PO3	PO4	PO5	PO 6	PO7	PO8	PO9	PO1 0	PO1 1	PO1 2	Level
18CS32CO1	Understand the operation of Field effect transistors by V-I characteristics	3	2	2						2		2	2	L2
18CS32CO2	Understand the operation amplifier application circuits	3	2	2						2		2	2	L2

18CS32CO3	Understand the fundamentals of logic gates through truth table	3	2	2						2		2	2	L2
18CS32CO4	Simplify Boolean equations by Karnaugh map and Quine MCClusky method to design combinational circuits	3	2	2						2		2	2	L4
18CS32CO5	Design data processing circuits using combination of gates	3	2	2						2		2	2	L4
18CS32CO6	Understand the fundamentals of flip flops by truth table and timing diagram	3	2	2						2		2	2	L2
18CS32CO7	Represent the flip flops as state diagram, characteristic equation	2		2										L2
18CS32CO8	Illustrate the register and counter properties through truth table and timing diagram	3		2						2		2	2	L2
18CS32CO9	Design of mod n counters by combination of flip flops	3		2						2		2	2	L4
18CS32C10	Interpret data conversion techniques through counter, continuous , dual slop methods	2		2						2		2	2	L2
Note: Mention the mapping strength as 1, 2, or 3														

4. Mapping Justification

Mapping		Justification	Mapping Level
CO	**PO**	**-**	**-**
CO1	PO1	Knowledge of FET is required in amplifier circuits which are used in complex circuits like transmitters and receivers	3
CO1	PO2	Analysing problem in amplifier circuits require knowledge of FETs	2
CO1	PO3	FETs are used in testing devices like oscilloscopes , voltmeters	2
CO1	PO4	No investigations and interpretation content no mapping	
CO1	PO5	No content tool, no mapping	
CO1	PO6	No engineering practice	
CO1	PO7	No matching for environment and sustainability	
CO1	PO8	No matching for ethical principles	
CO1	PO9	3	
CO1	PO10	No communication	
CO1	PO11	For project development in area of embedded devices, electronic projects knowledge of FET is useful	2
CO1	PO12	Learning in the context of technology changes .	2
CO2	PO1	Opamps are used in baseband receivers ,signal generators etc	3
CO2	PO2	Knowledge is useful in analysis of communication circuits	2
CO2	PO3	Opamps are used in circuits to perform mathematical operations	2
CO2	PO4	No investigations and interpretation content no mapping	
CO2	PO5	No content tool, no mapping	
CO2	PO6	No engineering practice	
CO2	PO7	No matching for environment and sustainability	
CO2	PO8	No matching for ethical principles	
CO2	PO9	For managing the analog circuits in communication individual should require the knowledge of opamps	2
CO2	PO10	No communication	
CO2	PO11	For project development in area of embedded devices, electronic projects knowledge of opamp is useful	2
CO2	PO12	Learning in the context of technology changes .practice	2

CO3	PO1	logic gates are used in all electronic devices like computers, lifts etc	3
CO3	PO2	knowledge of logic gates is required for analyzing problems in digital circuits	2
CO3	PO3	For designing digital circuits knowledge of logic gates is required	2
CO3	PO4	No investigations and interpretation content no mapping	
CO3	PO5	No content tool, no mapping	
CO3	PO6	No engineering practice	
CO3	PO7	No matching for environment and sustainability	
CO3	PO8	No matching for ethical principles	
CO3	PO9	For managing the digital circuits individual should require the knowledge of logic gates	2
CO3	PO10	No communication	
CO3	PO11	For electronic digital projects knowledge of logic gates is required	2
CO3	PO12	Learning in the context of technology changes .	2
CO4	PO1	Knowledge of K maps helps the students in circuit designing	3
CO4	PO2	Analysis of circuits makes the students better understanding of digital circuits	2
CO4	PO3	Helps the students in design of simple circuits using gates	2
CO4	PO4	No investigations and interpretation content no mapping	
CO4	PO5	No content tool, no mapping	
CO4	PO6	No engineering practice	
CO4	PO7	No matching for environment and sustainability	
CO4	PO8	No matching for ethical principles	
CO4	PO9	For developing the digital circuits with minimum gates simplification methods are useful for individual	2
CO4	PO10	No communication	
CO4	PO11	For digital project development simplification methods are useful	2
CO4	PO12	Learning in the context of technology changes .	2
CO5	PO1	Data processing circuits like mux ,demux are used in communication systems	
CO5	PO2	To analyze the problem in communication systems knowledge of data processing circuits is required	
CO5	PO3	Encoders and decoders are used in data communication	
CO5	PO4	No investigations and interpretation content no mapping	
CO5	PO5	No content tool, no mapping	
CO5	PO6	No engineering practice	
CO5	PO7	No matching for environment and sustainability	
CO5	PO8	No matching for ethical principles	
CO5	PO9	To manage the digital communication circuits knowledge of data processing circuits is useful	
CO5	PO10	No communication	
CO5	PO11	For digital project development knowledge of data processing circuits is useful	
CO5	PO12	Learning in the context of technology changes .	
CO6	PO1	Flip flops are basic components of registers which are used in building memory devices	3
CO6	PO2	To analyze the memory of sequential circuits knowledge of flip flops is required	2
CO6	PO3	Design of sequential circuits needs the knowledge of flip flops	2
CO6	PO4	No investigations and interpretation content no mapping	
CO6	PO5	No content tool, no mapping	
CO6	PO6	No engineering practice	

CO6	PO7	No matching for environment and sustainability	
CO6	PO8	No matching for ethical principles	
CO6	PO9	To manage the memory in sequential circuits individual require the knowledge of flipflops	2
CO6	PO10	No communication	
CO6	PO11	For digital electronic projects having memory knowledge of flip flop is required	2
CO6	PO12	Learning in the context of technology changes .	2
CO7	PO1	Flip flop representation is required in design of counters	2
CO7	PO2	No analysis. No mapping	
CO7	PO3	For digital clock design flip flop representation is required	2
CO7	PO4	No investigations and interpretation content no mapping	
CO7	PO5	No content tool, no mapping	
CO7	PO6	No engineering practice	
CO7	PO7	No matching for environment and sustainability	
CO7	PO8	No matching for ethical principles	
CO7	PO9	No team work	
CO7	PO10	No communication	
CO7	PO11	No project development	
CO7	PO12	No lifelong learning .	
CO8	PO1	Register and counters are sequential logic circuits which are used to construct Finite state machines, a basic building block in all digital circuitry.	3
CO8	PO2	No analysis	
CO8	PO3	Registers are used in design of memory devices	2
CO8	PO4	No investigations and interpretation content no mapping	
CO8	PO5	No content tool, no mapping	
CO8	PO6	No engineering practice	
CO8	PO7	No matching for environment and sustainability	
CO8	PO8	No matching for ethical principles	
CO8	PO9	For storing and managing the data in memory individual should require the knowledge of registers	2
CO8	PO10	No communication	
CO8	PO11	Every applications requires memory to store the data and knowledge of registers is required	2
CO8	PO12	lifelong learning & understanding the sequential circuits is essential for digital design	2
CO9	PO1	Counters are basic components of digital clock	3
CO9	PO2	No analysis	
CO9	PO3	For most of digital applications clock is used	2
CO9	PO4	No investigations and interpretation content no mapping	
CO9	PO5	No content tool, no mapping	
CO9	PO6	No engineering practice	
CO9	PO7	No matching for environment and sustainability	
CO9	PO8	No matching for ethical principles	
CO9	PO9	For designing of digital clock individual require th knowledge o design of counters	2
CO9	PO10	No communication	
CO9	PO11	For electronic projects counter design is useful for dsigning the digital clock	2
CO9	PO12	Learning in the context of technology changes	2

CO10	PO1	Knowledge of ADC and DAC are required building in Broadband communications systems ,Satellite Communications , Radars and jammers	3
CO10	PO2	No analysis	
CO10	PO3	For data conversion in electronic applications knowledge of ADC and DAC is required	2
CO10	PO4	No investigations and interpretation content no mapping	
CO10	PO5	No content tool, no mapping	
CO10	PO6	No engineering practice	
CO10	PO7	No matching for environment and sustainability	
CO10	PO8	No matching for ethical principles	
CO10	PO9	For applications which involve data conversion individual require the knowledge of data convertes	2
CO10	PO10	No communication	
CO10	PO11	For digital electronic projects knowledge of ADC and DAC is required for convert data fron analog to digital or digital to analog	2
CO10	PO12	Learning in the context of technology changes	2

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Mod	Title	Teaching	No. of question in Exam	CO	Levels

CS
Prepared by Checked by Approved

ule #		Hours	CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	Field effect transistors and operation amplifiers	11		-	4	1	1	2	CO1, CO2	L2
2	Combinational logic circuits	10	2	-	-	1	1	2	CO3, CO4	L2, L4
3	Data processing circuits and flip flops	11	2		-	1	1	2	CO5, CO6	L2, L4
4	Register and counters	10	-	2	-	1	1	2	CO7, C08	L2
5	Counter design and data converters	10	-	2	4	1	1	2	CO9, CO10	L2, L4
-	**Total**	**52**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

Note: Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	30	CO3, CO4 ,CO5, CO6	L2, l4
CIA Exam – 2	30	CO7, C08,CO9, CO10	L2, L4
CIA Exam – 3	30	CO1, CO2	L2
Assignment - 1	10	CO3, CO4 ,CO5, CO6	L2, L4
Assignment - 2	10	CO7, C08,CO9, CO10	L2, L4
Assignment - 3	0	CO1, CO2	L2
Seminar - 1	0	CO3, CO4 ,CO5, CO6	L2, L4
Seminar - 2	0	CO7, C08,CO9, CO10	L2, L4
Seminar - 3	10	CO1, CO2	L2
Other Activities – define – Slip test		CO1 to C10	L2, L3, L4
Final CIA Marks	**40**	**-**	**-**

Note : Blooms Level in last column shall match with A.2 above.

D1. TEACHING PLAN - 1

Module - 2

Title:	Combinational logic circuits	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand the fundamentals of logic gates through truth table	CO1	L2
2	Simplify Boolean equations by Karnaugh map and Quine MCClusky method to design combinational circuits	CO2	L4
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction to Subject, course objectives and outcomes	C03	L2
2	The Basic Gates: Review of Basic Logic gates,,	C03	L2
3	Introduction to HDL. Positive and Negative Logic	CO3	L2
4	Combinational Logic Circuits: Sum-of-Products Method	CO4	L2
5	Truth Table to Karnaugh Map,	CO4	L2
6	Pairs ,Quads, and Octets, Karnaugh Simplifications,	CO4	L2
7	Don't-care Conditions,	CO4	L2
8	Product-of-sums Method, Product-of-sums simplifications,	CO4	L4

9	Simplification by Quine- McClusky Method,	CO4	L4
10	Hazards and Hazard covers, HDL Implementation Models.	CO4	L2
		CO4	
c	**Application Areas**	**CO**	**Level**
1	Use of logic gates for building combinational circuits	CO3	L2
2	Used to simplification of boolean expressions	CO4	L4
d	**Review Questions**	-	-
1	Explain the logic circuit and truth table of the Inverter, OR and AND gate	CO1	L1
2	Why NAND & NOR gates are called universal gates.	CO1	L3
3	Differentiate between positive and negative logic.	CO2	L2
4	Implement AB+CD with only three NAND gates. Draw logic diagram also. Assume the inverted input is available.	CO2	L4
5	Minimize the following using K-maps: if(A,B,C,D)=Σm(0,1,2,3,5,9,14,15)+ΣΦ(4,8,11,12)	CO2	L2
6	Derive minimal SOP expression using K map and draw circuit diagram f(a,b,c,d) = Σm(1,4,6,8,9,10,11,12,13)+d(3,15)	CO2	L5
7	Derive minimal POS expression using K map and draw circuit diagram f(a,b,c,d) = πM(1,2,8,9,12,13,14)+d(0,14,15)	CO2	L2
8	What is static-1 hazard? Explain with an example how it can be covered.	CO2	L3
9	Simplify the given expression using Quine Mcclusky method f(a,b,c,d)= Σm(1,2,8,9,12,13,14)	CO2	L4
		CO1	L1
e	**Experiences**	-	-
1		CO1	L2
2			
3			
4		CO3	L3
5			

Module – 3

Title:	Data processing circuits	Appr Time:	11 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Design data processing circuits using combination of gates	CO5	L4
2	Understand the fundamentals of flip flops by truth table and timing diagram	CO6	L2
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
11	Data Processing Circuits: Multiplexers, Demultiplexer	CO5	L4
12	1-of-16 Decoder, BCD to Decimal Decoders	CO5	L4
13	Seven Segment Decoders, Encoders	CO5	L4
14	Exclusive-OR Gates, Parity Generators and Checkers,	CO5	L4
15	Magnitude Comparator, Prog rammable Array Logic	CO5	L4
16	Programmable Logic Arrays, HDL Implementation of Data Processing Circuits.	CO5	L4
17	Arithmetic Building Blocks, Arithmetic Logic Unit	CO5	L4
18	Flip- Flops: RS Flip-Flops,	CO6	L2
19	Gated Flip-Flops, Edge-triggered RS FLIP-FLOP,	CO6	L2
20	Edge-triggered D FLIP-FLOPs,	CO6	L2
21	Edge-triggered JK FLIP-FLOPs.	CO6	L2

c	**Application Areas**	**CO**	**Level**
1	Data processing circuits can be used in communication system	CO5	L4
2	Flip flops are used to store the data	CO6	L2
d	**Review Questions**	-	-
1	Why is a Multiplexer called a Universal logic	CO5	L2
2	Configure 16 to 1 MUX using 4 to 1 MUX	CO5	L4
3	Implement the f(x,y,z)= Σm(0,4,5,6) function using 8to1 MUX	CO5	L4
4	Define parity generator and parity checker	CO5	L2
5	Design 3 - 8 decoder	CO5	L4
6	Design a 32 to 1 multiplexer using two 16 to 1 multiplexers and one 2 to 1 multiplexer.	CO5	L4
7	Give seven segment decoder using PLA.		
8	Design Decimal to BCD encoder.	CO5	L4
9	Explain RS and Gated Flip Flops.	CO6	L2
10	Explain edge triggered D and JK Flip Flops	CO6	L2
e	**Experiences**	-	-
1			
2			
3			
4			
5			

E1. CIA EXAM – 1

a. Model Question Paper - 1

Crs Code:	18CS32	Sem:	III	Marks:	30	Time:	75 minutes
Course:	Analog and Digital circuits						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain the logic circuit and truth table of the Inverter, OR and AND gate	5	CO3	L2
	b	What is static-1 hazard? Explain with an example how it can be covered.	5	CO4	L2
	c	Minimize the following using K-maps: if(A,B,C,D)=Σm(0,1,2,3,5,9,14,15)+d(4,8,11,12)	5	CO4	L4
		OR			
2	a	Implement AB+CD with only three NAND gates. Draw logic diagram also. Assume the inverted input is available.	4	CO3	L2
	b	Derive minimal POS expression using K map and draw circuit diagram f(a,b,c,d) = Σm(1,4,6,8,9,10,11,12,13)+d(3,15)	5	CO3	L4
	c	Simplify the given expression using Quine Mcclusky method f(a,b,c,d)= Σm(1,2,8,9,12,13,14)	6	CO4	L4
		OR			
3	a	Configure 16 to 1 MUX using 4 to 1 MUX	5	CO5	L4
	b	Implement the f(w,x,y,z)= Σm(0,4,5,6,9,10)function using 8to1 MUX	5	CO5	L4
	c	Explain Edge triggered JK Flip Flops.	5	CO6	L2
4	a	Design a 32 to 1 multiplexer using two 16 to 1 multiplexers and one 2 to 1 multiplexer.	5	CO5	L4
	c	Design Decimal to BCD encoder.	5	CO5	L4
	d	Explain edge triggered D Flip Flops	5	CO6	L2

b. Assignment -1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	CS501PC	Sem:	I	Marks:	5 / 10	Time:	90 – 120 minutes
Course:	Analog and Digital circuits						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	USN	Assignment Description	Marks	CO	Level
1		Explain the logic circuit and truth table of the Inverter, OR and AND gate	6	CO3	L2
2		Why NAND & NOR gates are called universal gates. Convert NAND gates into Inverter,OR and And gates	5	CO3	L2
3		Differentiate between positive and negative logic.	5	CO3	L2
4		Implement AB+CD with only three NAND gates. Draw logic diagram also. Assume the inverted input is available.	4	CO3	L2
5		Minimize the following using K-maps: if(A,B,C,D)=Σm(0,1,2,3,5,9,14,15)+d(4,8,11,12)	6	CO4	L4
6		Derive minimal SOP expression using K map and draw circuit diagram f(a,b,c,d) = Σm(1,4,6,8,9,10,11,12,13)+d(3,15)	6	CO4	L4
7		Derive minimal POS expression using K map and draw circuit diagram f(a,b,c,d) = πM(1,2,8,9,12,13,14)+d(0,14,15)	6	CO4	L2
8		What is static-1 hazard? Explain with an example how it can be covered.	6	CO4	L2
9		Simplify the given expression using Quine Mcclusky method f(a,b,c,d)= Σm(1,2,8,9,12,13,14)	8	CO4	L4
10		Simplify the given expression using Quine Mcclusky method f(a,b,c,d)= Σm(1,2,8,9,12,13,14)	8	CO4	L4
11		Configure 16 to 1 MUX using 4 to 1 MUX	5	CO5	L4
12		Implement the f(x,y,z)= Σm(0,4,5,6)function using8to1 MUX	5	CO5	L4
13		Define parity generator and parity checker	5	CO5	L4
14		.Design 3 - 8 decoder	5	CO5	L4
15		Design a 32 to 1 multiplexer using two 16 to 1 multiplexers and one 2 to 1 multiplexer.	5	CO5	L4
16		Design seven segment decoder using PLA.	6	CO5	L2
17		Design Decimal to BCD encoder.	8	CO5	L4
18		Explain edge triggered D and JK Flip Flops	6	CO6	L2

D2. TEACHING PLAN - 2

Module – 4

Title:	Register and counters	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Represent the flip flops as state diagram, characteristic equation	CO7	L2
2	Illustrate the register and counter properties through truth table and timing diagram	CO8	L2
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Flip-Flops: FLIP-FLOP Timing, JK Master-slave FLIP-FLOP,	CO7	L2
2	Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs	CO7	L2
3	HDL Implementation of FLIP-FLOP. ,	CO7	L2
4	Registers: Types of Registers:Serial In - Serial Out, Serial In - Parallel out,	CO8	L2
5	Parallel In - Serial Out, Parallel In - Parallel Out,	CO8	L2

6	Universal Shift Register, Applications of Shift Registers,	CO8	L2
7	Register implementation in HDL	CO8	L2
8	Counters: Asynchronous Counters,	CO8	L2
9	Decoding Gates, Synchronous Counters,	CO8	L2
10	Changing the Counter Modulus.	CO8	L2
c	**Application Areas**	**CO**	**Level**
1	Flip flops can be used as frequency divider	CO7	L2
2	Registers are used to store the instructions	CO8	L2
d	**Review Questions**	-	-
1	Mention the difference between combinational & sequential circuits with block diagram.	CO1	L2
2	Explain the operation of Jk master slave flip flop flip-flop. With logic diagram,characteristic table	CO7	L2
3	Explain the working of switch contact bounce circuit	CO7	L2
4	Derive the characteristic equation of RS JK and D flip flop	CO7	L2
5	Draw the state diagram of RS JK and D flip flop		
6	List the different types of registers		
7	Explain the serial in serial out shift register . Show how the data is entered for data 1010		
8	Briefly explain the applications of registers		
9	Explain the ring counters and Johnson countesr		
10	Differentiate synchronous and asynchronous counters		
11	Explain the asynchronous mod 8 countes		
e	**Experiences**	-	-
1			
2			
3			
4			
5			

Module – 5

Title:	Counter design and data converters	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Design of mod n counters by combination of flip flops	CO9	L4
2	Interpret data conversion techniques through counter, continuous , dual slop methods	C10	L2
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Counters: Decade Counters, Presettable Counters	CO9	L2
2	Counter Design as a Synthesis problem,	CO9	L4
3	A Digital Clock,	CO9	L4
4	Counter Design using HDL	CO9	L3
5	D/A Conversion and A/D Conversion: Variable, Resistor Networks,	C10	L2
6	Binary Ladders, D/A Converters,	C10	L2
7	D/A Accuracy and Resolution,	C10	L2
8	A/D Converter-Simultaneous Conversion	C10	L2
9	A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques,	C10	L2

10	Dual-slope A/D Conversion, A/D Accuracy AND RESOLUTTION	C10	L2
c	**Application Areas**	**CO**	**Level**
1	Counters are used for counting electronic pulses	CO9	L4
2	Used to convert signals	C10	L2
d	**Review Questions**	-	-
1	Explain how decade counter works	CO7	L2
2	What are presettable counters	CO7	L2
3	Write block diagram of digital clock	CO8	L2
4	Design mod 6 counter using D flip flop	CO7	L4
5	Explain binary ladders	CO8	L2
6	Explain counter method for data conversion	CO8	L2
e	**Experiences**	-	-
1			
2			
3			
4			
5			

E2. CIA EXAM – 2

a. Model Question Paper - 2

Crs Code:	18CS32	Sem:	III	Marks:	30	Time:	75 minutes		
Course:	Analog and Digital Electronics								
-	**-**	**Note: Answer any 2 questions, each carry equal marks.**					**Marks**	**CO**	**Level**
1	a	With a neat logic diagrams and truth table. Explain the working of JK master slave Flip-Flop along with its implementation using NAND Gates.					7	Co7	L2
	b	Derive the characteristic equation and state diagramfor SR, D and JK Flip-Flop.					8	CO7	L2
		OR							
2	a	Explain 4 bit serial in parallel out register.					6	CO8	L2
	b	Explain a 3 bit binary Ripple up counter. Give the block diagram, truth table and output					7	CO8	L2
	c	Differentiate between synchronous counter and asynchronous counters					2	CO8	L2
3	a	Design synchronous MOD — 6 counter with truth table and state diagram.					7	CO9	L4
	b	Design the digital clock					8	CO8	L4
		OR							
4	a	Explain 5 bit Resistor divider with diagram.					5	C10	L2
	b	Explain the terms Accuracy and Resolution for D/A converter					4	C10	L2
	c	Explain with Block diagram the operation of successive approximation converter					6	C10	L2

b. Assignment – 2

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	CS501PC	Sem:	3	Marks:	5 / 10	Time:	90 – 120 minutes
Course:	Analog and Digital Electronics						

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1		Explain the working of JK master slave Flip Flop along with implementation using NAND gates	6	CO7	L2
2		Draw the stare diagram of JK, D and SR flipflop	6	CO7	L2
3		Explain 4 bit serial in serial out register	6	CO7	L2
4		Write the comparison between Synchronous and Asynchronous counter.	4	CO8	L2
5		Explain a 3 bit binary Ripple up counter. Give the block diagram, truth table and output	6	CO8	L2
6		What is universal shift Register'? Explain any one application of universal shift register with block diagram and truth tab	6	CO8	L2
7		What is a shift register? Explain how shift register can be used as a serial adder	8	CO8	L2
8		Design mod 7 counter using JK Flipflop	8	CO9	L4
9		With neat diagram explain the working of digital clock	8	CO9	L2
10		Explain 2 bit simultaneous A/D converter...	6	C10	L2
11		What is Binary Ladder? Explain the Binary Ladder with Digital input of 1000	6	C10	L2
12		Explain 5 bit Resistor divider with diagram.	6	C10	L2
13		Explain the terms Accuracy and Resolution for D/A converter.	4	C10	L2
14		Explain with Block diagram the operation of successive approximation converter	8	C10	L2
15		Explain counter type A/D converter with diagram.	6	C10	L2
16					
33					
47					

D3. TEACHING PLAN - 3

Module – 1

Title:	Field effect transistors and Operational amplifier	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand the operation of Field effect transistors by V-I characteristics	CO1	L2
2	Understand the operation amplifier application circuits	CO2	L2
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Field Effect Transistors: Junction Field Effect Transistors, MOSFETs	CO1	L2
2	Differences between JFETs and MOSFETs	CO1	L2
3	Biasing MOSFETs, FET Applications, CMOS Devices.	CO1	L2
4	Wave-Shaping Circuits: Integrated Circuit(IC) Multi vibrators.	CO1	L2
5	Introduction to Operational Amplifier: Ideal v/s practical Opamp, Performance Parameters	CO2	L2
6	Amplifier Application Circuits :Peak Detector Circuit	CO2	L2
7	Comparator, Active Filters,	CO2	L2
8	Non-Linear Amplifier, Relaxation Oscillator	CO2	L2
9	Current-To-Voltage Converte	CO2	L2
10	Voltage-To-Current Converter.	CO2	L2
c	**Application Areas**	**CO**	**Level**
1	FETs are used as analog switches, amplifiers and current limiters	CO1	L2

2	Opamps are used for current to voltage converter, integrator	CO2	L2
d	**Review Questions**	-	-
1	Explain the working of CMOS, with its power consumption properties?	CO1	L2
2	Explain construction and principle of operation of JFET along with its drain and trans-conductance characteristics?	CO1	L2
3	Explain construction and principle of operation of D-MOSFET along with its drain and trans- conductance characteristics?	CO1	L2
4	Explain construction and principle of operation of E-MOSFET along with its drain and trans- conductance characteristics?	CO1	L2
5	Write the differences between JFETs and MOSFETs.	CO1	L2
6	What is differences b/w ideal and practical op-amp amplifier?	CO2	L2
7	Explain astable multivibrator using 555 timer?	CO1	L2
8	Explain mono multivibrator using 555 timer?	CO1	L2
9	Explain Comparator? How do you convert sine wave to rectangular output, using Op-Amp?	CO2	L2
10	Explain the CMRR, Slew rate, PSRR and gain-bandwidth performance parameter of a practical op- amp?	CO2	L2
e	**Experiences**	-	-
1		CO10	L2
2			
3			
4		CO9	L3
5			

E3. CIA EXAM – 3

a. Model Question Paper - 3

Crs Code:	18CS32	Sem:	3	Marks:	30	Time:	75 minutes
Course:	Analog and Digital Electronics						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain the working of CMOS, with its power consumption properties?	05	CO1	L2
	b	Explain construction and principle of operation of JFET along with its drain and trans-conductance characteristics?	10	CO1	L2
		or			
2	a	Explain astable multivibrator using 555 timer?	10	CO1	L2
	b	What is differences b/w ideal and practical op-amp amplifier?	05	CO2	L2
3	a	Explain construction and principle of operation of D-MOSFET along with its drain and trans- conductance characteristics?	05	CO1	L2
	b	Write the difference between JFET and MOSFET	05	CO1	L2
	c	Distinguish between Bistable, Monostable and Astable Multivibrator.	05	CO1	L2
		or			
4	a	With a neat diagram explain op-amp Schmitt Trigger circuit?	07	CO2	L2
	b	Draw the circuit diagram of a current to voltage converter using opamps. What type of feedback is used in the circuit? What decides the maximum value of feedback resistance to be used in the circuit?	08	CO2	L2

b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	CS501PC	Sem:	III	Marks:	5 / 10	Time:	90 – 120 minutes
Course:	Analog and Digital Electronics						

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1		Draw the cross-sectional view of an N channel JFET and explain its principle of operation, Draw the Ig vs Vds graph for different values of Vgs and highlight the different regions of operation.	6	Co1	L2
2		Draw the circuit for voltage divider configuration for E-MOSFET.	6	CO1	L2
3		Explain Comparator? How do you convert sine wave to rectangular output, using Op-Amp?	6	Co2	L2
4		Define slew rate of Op–Amp. (ii) Determine the cutoff frequency of OP–amp whose unity gain bandwidth is 1 MHz and open loop gain is 2 x 10^5. (iii) List the expression for the output of non– inverting amplifier and inverting op-amp amplifier	6	Co2	L2
5		What is an peak detector & absolute value circuit? Explain the functional principal, with the circuit?	8	CO2	L2
6		Draw the circuit diagram of a current to voltage converter using opamps. What type of feedback is used in the circuit? What decides the maximum value of feedback resistance to be used in the circuit?	8	CO2	L2
7		What are the requirement of good Instrumentation Amplifier.	8	CO2	L2
8		What is an absolute value circuit? Explain the functional principal, with the circuit?	8	CO2	L2
9		Explain construction and principle of operation of n-channel JFET along with its drain and trans-conductance characteristics?	8	CO1	L2
10		Explain construction and principle of operation of p-channel JFET along with its drain and trans-conductance characteristics?	6	CO1	L2

F. EXAM PREPARATION

1. University Model Question Paper

Course:	Analog and Digital Electronics					Month / Year	/2018	
Crs Code:	18CS32	Sem:	3	Marks:	100	Time:	180 minutes	
-	**Note**	Answer all FIVE full questions. All questions carry equal marks.				**Marks**	**CO**	**Level**
1	a	Explain the construction & working and principle of operation of an n-channel JFET.				10	CO1	L2
	b	What are the differences between JFET & MOSFET.				04	CO1	L2
	c	What is differences b/w ideal and practical op-amp amplifier?				06	CO2	L2
		OR						
-	a	Explain with neat sketches the operation and characteristics of N-channel DE-MOSFET				10	CO1	L2
	b	Explain the working of a CMOS inverter.				10	CO1	L2
2	a	What are Universal gates? Implement the basic gates using Universal gates only.				10	C03	L2
	b	Using K-map find the reduced SOP form of f(A,B,C,D)=ΣM(5,6,7,12,13)+Σd(4,9,14,15).				10	CO4	L4
		OR						
-	a	Explain Duality Theorem?				04	CO3	L2
	b	Write the verilog code for given expression. Y=AB+CD				04	CO4	L4
	c	Simplify the following using Mc-Cluskey method f=ΣM(4,8,10,11,12,15)+d(9,14)				12	CO4	L4

CS
Prepared by Checked by Approved

3	a	Implement the following function using a 8:1 multiplexer: f(a,b,c,)= ΣM(0,1,3,4).	10	CO5	L4
	b	What is a magnitude comparator? Explain with a neat block diagram an n-bit magnitude comparator	05	CO5	L4
	c	Design 7 segment decoder using PLA	05	CO6	L2
		OR			
-	a	Realize the following function using the 3:8 decoder F_1(A, B, C)= ΣM(1,2,3,4), F_2(A, B, C)= ΣM(3,5,7).	10	CO5	L4
	b	Give transition diagram of JK and T Flip flops	06	CO6	L2
	c	Differentiate between combinational circuit and sequential circuit	04	CO6	L2
4	a	Draw the logic diagram of a 4-bit serial in serial out shift register using J-K flip flop and explain.	10	CO8	L2
	b	Design a modulo-5 up counter (synchronous) using J-K flip flop	10	CO8	L4
		OR			
-	a	Explain Johnson Counter with neat diagram and timing diagram	10	CO7	L4
	b	Difference between Asynchronous and Synchronous Counter	04	CO8	L2
	c	Draw the logic circuits and the excitation tables for the T, JK flip-flops.	06	CO7	L4
5	a	Explain with logic diagram 3 bit simultaneous A/D converters.	10	CO10	L4
	b	What is Binary ladder? Explain the binary ladder with digital input of 1000	10	CO10	L4
		OR			
	a	Give performance parameters of DAC or D/A converters	10	CO10	L4
	b	Explain Digital clock with block Diagram.	10	CO9	L4
-					

2. SEE Important Questions

Course:		Analog and digital Electronics					Month / Year	August /2018	
Crs Code:		18CS32	Sem:	3	Marks:	100	Time:	180 minutes	
	Note	Answer all FIVE full questions. All questions carry equal marks.					-	-	
Module	Qno.	Important Question					**Marks**	**CO**	**Year**
1	1	Explain with the help of a circuit diagram and characteristics curves working of N-channel E MOSFET					10	CO1	2017
	2	List and explain any one application of FET and its working with circuit diagram?					8	CO1	2017
	3	Explain the performance parameters of Op Amp					10	CO2	2017
	4	How CMOS can be used as inverting switch					6	CO1	2017
	5	Mention and explain the working of any two application of Op Amp					8	CO2	2017
2	1	Minimize the following using K-maps: I)SOP expression given by f(A,B,C,D) = Σm (6,7,9,10,13) + d(1,4,5,11) ii) POS expression given by f(A,B,C,D) =ΠM(1,2,3,4,10)+ d(0,15)					8	CO4	2017
	2	Describe positive and negative logic. List the equivalences between them					6	CO3	2017
	3	Minimize the following using K-maps: if(A,B,C,D)=Σm(5,6,7,12,13)+d(4,9,14,15)						CO4	2017
	4	Define hazard. Explain different types of hazard					8	CO4	2017

CS
Prepared by Checked by Approved

	5	Simplify the given expression using Quine Mcclusky method f(a,b,c,d)= Σm(0,1,2,3,10,11,12,13,14,15)	10	CO4	2017
3	1	Implement the following function using 8:1 multiplexer f(a,b,c,d) = Σm(0,1,5,6,8,10,12,15)	8	CO5	2017
	2	Design 7- segment decoder using PLA	8	CO5	2017
	3	What is magnitude comparator? Explain 1 bit magnitude comparator	6	CO5	2017
	4	What is Multiplexer? Design 32 to 1 MUX using two 16 to 1 and one 2 to 1 MUX	6	CO5	2017
	5	Differentiate between combinational and sequential circuit	4	CO6	2017
4	1	With block diagram and truth table explain the working of JK master slave Flip flop	8	CO7	2017
	2	With neat diagram explain ring counter	6	CO8	2017
	3	Compare synchronous and asynchronous counter	4	CO8	2017
	4	What is shift register? With neat diagram, explain 4 bit parallel in serial out shift registers	8	CO8	2017
	5	Derive the characteristic equation for SR, D and JK flip flop	6	CO8	2017
5	1	Explain 2 bit simultaneous A/D converter	8	CO10	2017
	2	What is binary ladder? Explain the binary ladder with digital input of 1000	8	CO10	2017
	3	With neat diagram. Explain digital clock	10	CO9	2017
	4	Define counter. Design A synchronous counter for the sequence 0→4→1→2→6→0→4 using JK flip flop	12	CO9	2017
	5	Design Asynchronous counter for the sequence 0→4→1→2→6→0→4 using SR flip flop	12	CO9	2017